

Design of Ultra-Low-Power Systems
Professor Anantha Chandrakasan
Joseph F. and Nancy P. Keithley Professor of Electrical Engineering, MIT

Abstract:

Energy efficiency is a key design consideration in wireless systems. Energy efficient system design requires systematic optimization at all levels of the design abstraction ranging from process technology and logic design to architectures, algorithms and networking. The energy expended per operation continues to improve as the power supply voltages are scaled. Sub-threshold circuit design provides a major opportunity to dramatically reduce the power dissipation of digital integrated circuits. The opportunities and challenges associated with sub-threshold design will be presented. Idle-mode power (i.e., leakage) must also be carefully managed in sub-90nm CMOS and will require the use of techniques such as fine-grain power gating and ultra-dynamic voltage scaling. 3-D integration also presents an interesting opportunity for power savings – the potential power savings of this technology will be presented for a 3-D FPGA circuit. Specific examples of power management in integrated circuits will be presented, focusing on wireless sensor networks and impulse based ultra-wideband communications as drivers.

Biography:

Anantha P. Chandrakasan received the B.S, M.S. and Ph.D. degrees in Electrical Engineering and Computer Sciences from the University of California, Berkeley, in 1989, 1990, and 1994 respectively. Since September 1994, he has been with the Massachusetts Institute of Technology, Cambridge, where he is currently where he is currently the Joseph F. and Nancy P. Keithley Professor of Electrical Engineering.

He has received several awards including the 1993 IEEE Communications Society's Best Tutorial Paper Award, the IEEE Electron Devices Society's 1997 Paul Rappaport Award for the Best Paper in an EDS publication during 1997, the 1999 Design Automation Conference (DAC) Student Design Contest Award and the first place in the 2004 DAC/ISSCC Student Design Contest Award (operational category). He held the Analog Devices Career Development Chair from 1994 to 1997. He received the NSF Career Development award in 1995, the IBM Faculty Development award in 1995 and the National Semiconductor Faculty Development award in 1996 and 1997.

His research interests include micro-power digital and mixed-signal integrated circuit design, wireless microsensor system design, ultra-wideband radios, and emerging technologies. He is a co-author of Low Power Digital CMOS Design (Kluwer Academic Publishers, 1995) and Digital Integrated Circuits (Pearson Prentice-Hall, 2003, 2nd edition). He is also a co-editor of Low Power CMOS Design (IEEE Press, 1998), Design of High-Performance Microprocessor Circuits (IEEE Press, 2000), and Leakage in Nanometer CMOS Technologies (Springer, 2005).

He has served as a technical program co-chair for the 1997 ISLPED, VLSI Design '98, and the 1998 IEEE Workshop on Signal Processing Systems. He was the Signal Processing Sub-committee Chair for ISSCC 1999-2001, the Program Vice-Chair for ISSCC 2002, the Program Chair for ISSCC 2003, and the Technology Directions Sub-committee Chair for ISSCC 2004-2006. He is the Technology Directions Chair for ISSCC 2007. He was an Associate Editor for the IEEE Journal of Solid-State Circuits from 1998 to 2001. He serves on the SSCS AdCom and is the Meetings Committee Chair. He is a Fellow of the IEEE. He is an Associate Director of the Microsystems Technology Labs.